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PATENT

AMENDMENT D

REMARKS

Claims 1-57 remain rejected, now under 35 U.S.C. §103(a) as being unpatentable over Tripathi et al., U.S. Patent No. 5,974,089 ("Tripathi") in view of Beard, U.S. Patent No. 5,796,359 ("Beard"). This rejection is respectfully traversed and it is submitted that these claims recite subject matter which is patentable over Tripathi and Beard.

Regarding claims 1, 20 and 39, the Examiner correctly notes that Tripathi does not teach discrete time pulse width modulation (PWM) as presently recited. However, the Examiner then contends that Beard teaches providing discrete time PWM. In support of this, the Examiner cites Figures 1-2, column 2, line 8, column 3, lines 23-67, and column 4, lines 5-67, of Beard. While Figures 1-2, column 3, lines 23-67, and column 4, lines 5-67, of Beard do disclose PWM in general terms, the reference to column 2, line 8, of Beard is not understood since such portion of Beard neither discloses nor suggests anything related to PWM. While the word "discrete" does appear there, and again in at column 2, line 13, the use of the word "discrete" in such places is to identify the ADC circuitry as being discrete, i.e., separate, from the data processing circuitry also discussed there.

In any event, it is respectfully submitted that while the remaining portions of Beard cited by the Examiner do disclose PWM generally, such disclosure of PWM is not in terms, either explicit or implicit, of discrete time PWM. To the contrary, at column 4, line 46, through column 5, line 13, of Beard it is expressly taught that "digital feedback signal 28" has a pulse width which follows the "high logical valued comparator output signal 20" which, in turn, follows the difference between the analog signals 22, 34 at the input terminals 14, 16 of the comparator 12. Hence, "digital feedback signal 28" has a pulse width which is continuous, i.e., "pulse-width

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modulator 24" performs continuous PWM by generating a pulse width with a duration as long as the input signal is at a logical high value.

In contrast thereto, as expressly recited in the present claims, a discrete time PWM signal is generated and fed back. As is well known in the art, a discrete time PWM signal is not continuous in that the pulse width has discrete durations which are determined by the value of the input signal at each triggering edge of the clock signal. For example, in the case of a preferred embodiment of the presently claimed invention, as disclosed in Figure 4 and at page 5, lines 22-25, "multi-bit quantized signal 107" is converted to "discrete time PWM signal 109" by "discrete pulse-width modulator stage 108" which is clocked by the same clock signal 199 as "quantizer 106". Hence, the rising and falling edges of "discrete time PWM signal 109" will only occur at discrete points in time, i.e., coincident with the triggering clock edge.

Therefore, it is respectfully submitted that it would not have been obvious to one of ordinary skill in the art to combine the subject matter of Beard with that of Tripathi and, therefore, independent claims 1, 20 and 39 are patentable over Tripathi and Beard. Accordingly, it is further submitted that dependent claims 2-19, 21-38 and 40-57 are also patentable over Tripathi and Beard, particularly in view of the further limitations in these latter claims.

More particularly, regarding claims 3, 22 and 41, the Examiner states, with no supporting citation(s), that "the apparatus of Tripathi would include a feed forward circuit as to accurately analyze the modulator by modeling ideal quantization noise and other sources of non-ideal noise introduced by the feed forward ADC converter." This stated basis for this rejection appears to be identical to that presented for the previously cited Haga and Paul references, and just as discussed in Amendment D (and incorporated herein by reference), the source of the teaching or suggestion of such a motivation is not cited. Hence, it is respectfully submitted that it has not been

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adequately demonstrated how or why the subject matter of these claims is unpatentable over Tripathi and Beard.

Regarding claims 5, 24 and 43, the Examiner cites Figure 3 of Tripathi as teaching "at least one sampled integrator circuit". However, at column 6, lines 23-27, of Tripathi it is expressly stated that the integrators are "continuous-time integrators", i.e., not sampled.

Regarding claims 11, 29 and 30, the Examiner appears to cite column 4, lines 15-18, of Beard as teaching an "anti-aliasing stage". However, nowhere within column 4, lines 15-18, of Beard does the term "anti-aliasing" appear expressly or to be suggested.

Regarding claims 12, 31 and 50, the Examiner cites Figure 3 of Tripathi as disclosing the presently claimed subject matter. However, Figure 3 of Tripathi neither teaches nor suggests feeding back the quantized signal (e.g., the output of element 310 of Tripathi) as is expressly recited in these claims.

Regarding claims 19, 38, 56 and 57, the Examiner cites Figure 3 of Tripathi as disclosing the presently claimed subject matter. However, Figure 3 of Tripathi neither teaches nor suggests an "anti-aliasing stage".

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In the interests of expediting prosecution of this application, the Examiner is respectfully requested to contact the undersigned by telephone to discuss any further questions, comments or concerns.

Respectfully submitted,

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